REMARKS

Claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Tanaka et al., U.S. Patent No. 6,489,952. Further, claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hasegawa et al., U.S. Patent Application No. 2001/0011979. Applicants traverse these rejections because the references do not disclose or suggest a voltage offset to either a single positive or negative constant level at all times during operation, wherein the value of the offset has the *same polarity* at all times during operation except during signal application, and wherein the *offset is applied automatically* at all times during operation except during signal application, as recited in all amended independent claims 1, 3, 7, 8, 9, 12 and 17.

The present invention prevents decrease of contrast ratio caused by the incomplete memory effect (when data is maintained in a picture element), and in particular, is concerned with preventing light transmittance in the picture element when data pulses of zero amplitude for displaying "black" are applied to the element. The decrease of contrast ratio is prevented by the use of driving signals which are either positively or negatively offset a single, predetermined value with respect to a reference voltage of the panel, as shown in Figs. 4D1-4D6, which show potentials appearing across each picture element.

The amplitude of the single, offset value is selected depending on a desirable variation of contrast ratio of the display panel (page 14, lines 16-24). Once selected, the offset value does not change and is automatically applied. The offset

voltage is one constant value, and it can be either a positive or a negative value. The offset voltage does not change polarity, but is the same offset value at all times of operation when an offset is applied. For example, the single, constant offset value may be +1V at all time frames during operation where an offset is applied. Alternatively, the constant offset value may be –1V at all times during operation where an offset is applied. However, the offset value is not +1V for some frames, and –1V for other frames because the polarity is the same at all times.

In Tanaka et al., however, at least two offset values are used since the electrode of Tanaka et al. switches potential from negative to positive throughout the time of operation. Tanaka et al. teaches two offset values used as part of an inversion driving system, a system in which a direction of an electric field applied to a liquid crystal is inverted at every rewriting of a display screen. Tanaka et al. disclose two distinct levels, a positive level COM2 and a negative level COM1.

As shown in Figures 4-5 below, the COM1 signal line is driven alternately to the COM2 signal line, both lines being driven with an offset value for the purpose of making the voltage applied to the pixel close to zero. The offset alternates polarity corresponding to whether the odd line or the even line is driven for display. When the odd line is driven (S1, S3,...Sn-1), negative COM1 is applied. When the even line is driven (S2, S4,...Sn), positive COM2 is applied. Thus, the offset is sometimes negative (COM1) and sometimes positive (COM2) during each frame, depending on which line is driven. This process is disclosed at column 8, lines 46-58 of Tanaka et al.

FIG. 4

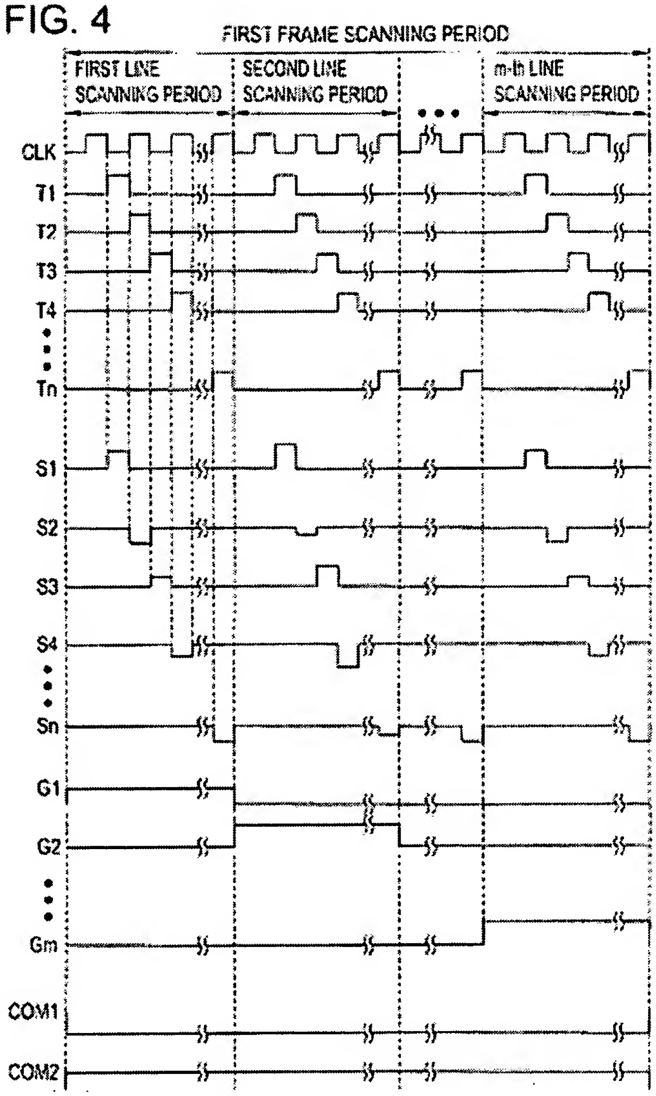
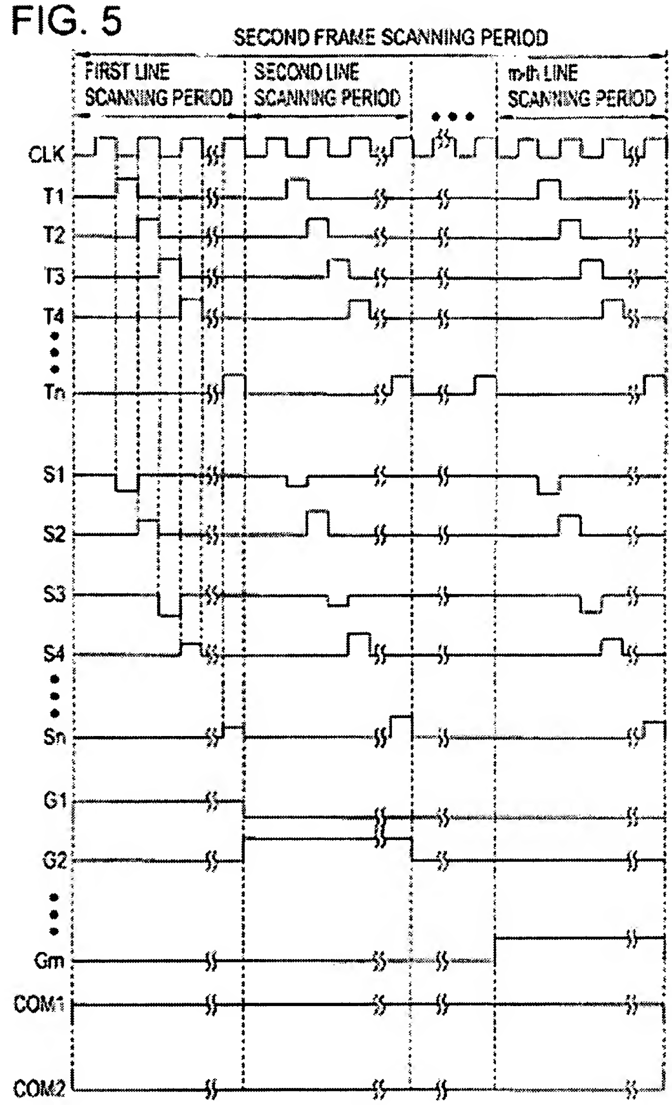


FIG. 5



In Figure 4, COM1 is negative and COM2 is positive, and in Figure 5, COM 1 is positive and COM2 is negative. COM1 and COM2 are alternately applied in this manner. For this reason, Tanaka et al. do not disclose or suggest a voltage offset to either a single, positive or negative constant level applied at all times during operation, wherein the value of the offset has the same polarity at all times. Withdrawal of the rejection based on Tanaka et al. is respectfully requested.

Hasegawa et al. does not disclose that "the offset is applied automatically at all times during operation except during signal application," as in the amended claims. In the present invention, the offset application is an automatic feature to prevent light transmittance in the picture element. In Hasegawa et al., the offset is applied during the "alignment treatment", which is only started by the user. At paragraph [0089] of Hasegawa et al., the procedure for initiating the alignment treatment is explained as follows:

> "An external switch 39 for starting/terminating the alignment treatment is provided in the liquid crystal display device 10 so that the alignment treatment can be started according to the determination of the user. When the user depresses the external switch, an alignment controller 36 and the alignment treatment for the liquid crystal is effected."

Thus, the alignment treatment, and therefore the offset, is not *automatically* applied at all times during operation, as in the amended claims. Further, the offset voltage of the alignment treatment is applied to a liquid crystal material during manufacturing or repair of a display, not during normal operation of the display, as recited in all independent claims of the present invention. In particular, the reference is directed to an alignment treatment for aligning the liquid crystal display, such as when the liquid crystal is destroyed by application of external forces. (paragraph [0088], [0090]).

Since the offset of Hasegawa is not automatically applied at all times during operation of the display, as required by all independent claims of the present invention, the rejection based on Hasegawa is traversed.

For the foregoing reasons, Applicants believe that this case is in condition for allowance, which is respectfully requested. The Examiner should call Applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

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April 12, 2006

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